NAME

Clara Schaertl Short — eclectical engineer working in silicon validation

SYNOPSIS

cu -c *+1(310)237-2826*
mail -s "Your resume" *clara@cshort.io*
curl *https://cshort.io/clarity.7* | **groff -mdoc** | **pstopdf**

DESCRIPTION

Clara Short (they/them or she/her) is a hardware engineer who *happens* to mostly write software these days: namely, tools for bringing up, validating, and using the new Design for Debug (DFD) features on the next generation of phone and laptop SoCs. In other words, they use their training as an EE to make hardware debugging easier for software engineers. Their favorite method of building trust with other teams is to start submitting pull requests for features their own team needs.

EXAMPLES

July 2019 - Present: Silicon Validation Engineer, Apple Inc., Cambridge, MA

- Responsible for silicon bringup and validation of Apple's cross-triggering network on each new SoC.
- Creates tools to extract DFD architecture information directly from the RTL design.
- Extends the OS kernel, boot loader, and SoC debugger to enable new validation and debug use cases.
- Trains triage engineers in tool usage and provides hands-on support during bringup and debug.
- Leads discussions with IP designers and software teams about future requirements.

May 2018 - August 2018: Silicon Validation Intern, Apple Inc., Austin, TX

- Wrote the collateral extraction tool for a new DFD feature, saving 20 engineering hours per stepping.
- Re-implemented SoC debugger support for the new feature to streamline collateral delivery.

June 2014 - December 2017: Control Systems Engineer, Mangan Inc., Long Beach, CA

- Designed and commissioned Programmable Logic Controller (PLC) systems in oil refineries.
- Created the client's standard software library for process analyzer PLCs.
- Introduced a tool for semi-automatic PLC software validation, saving 80 engineering hours per project.
- Independently managed projects up to $5,000.

May 2009 - May 2014: Submarine Officer, United States Navy, Kings Bay, GA

- Shift supervisor for operations, maintenance, and testing of a nuclear submarine with a crew of 160.
- Line manager for 12 electricians and electronics technicians.

COMPATIBILITY

Clara works best in a collaborative environment, where there's a culture of engineers regularly looking at each other's work and occasionally pairing on tricky problems. They prefer distributed, cross-functional organizations where accountability is everywhere but ‘‘ownership’’ is a dirty word - see above re: their habit of trading pull requests with other teams.

Remote work is a hard requirement for Clara, but they are willing to travel to the lab for hardware bringups (up to two weeks per quarter).

STANDARDS

- Fluent in Python and C; conversational in C++, `Tcl`(n), `sh`(1), and SystemVerilog.
- Uses JTAG, IEEE 1500, and Verdi NPI routinely; uses SQLite, GraphQL, and Xilinx FPGAs rarely.

HISTORY

August 2017 - May 2019: M.S. Electrical and Computer Engineering
University of Texas at Austin, Austin, TX.

June 2005 - May 2009: B.S. Electrical Engineering
United States Naval Academy, Annapolis, MD.