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# Clara Schaertl Short

## Education

May 2019 **M.S., Electrical and Computer Engineering** (Integrated Circuits and Systems), *University of Texas at Austin*, Austin, TX.
- Selected courses: Design for Low-Power and Robustness, High-Speed Computer Arithmetic, Verification of Digital Systems, Real-Time Operating Systems, VLSI CAD and Optimization.
- Technologies used: C, Tcl, SystemVerilog, HSPICE, Synopsys (DC/ICC/PrimeTime).

May 2009 **B.S., Electrical Engineering**, *United States Naval Academy*, Annapolis, MD.
- Honors: Tau Beta Pi.

## Work Experience

May 2018–Aug. 2018 **Intern, Silicon Validation** (Debug and Regression), *Apple Inc.*, Austin, TX.
- Developed automatic collateral generation tools for a new SoC debug feature, saving 10-20 hours of engineering effort per stepping.
- Streamlined existing SoC debug tools to support faster collateral delivery.
- Technologies used: Python, C++, Tcl, Bash, SQLite.

June 2014–Dec. 2017 **Control Systems Engineer**, *Mangan Inc.*, Long Beach, CA.
- Instrumentation, controls, and functional safety engineering in oil refineries.
- Introduced a tool for semi-automatic PLC software validation and obtained client buy-in for its use with safety-critical systems, saving 80-100 hours of engineering effort per project.
- Reverse engineered a complex legacy control system for six gasoline blender analyzers, designed its replacement, and developed the client's standard library for analyzer PLCs.
- Independently managed projects up to $5,000 as the client's single point of contact.
- Technologies used: Allen Bradley (PLC/SLC/CLX), Honeywell (TDC 3000), Triconex.

May 2009–May 2014 **Submarine Officer**, *United States Navy*, Kings Bay, GA/Atlantic Ocean.
- Shift supervisor for day-to-day operations, maintenance, and testing of a ballistic-missile submarine with a crew of 160. Line manager for 12 electricians and electronics technicians.

## Publications

In Review "Performance evaluation of a sum error detection scheme for mixed binary/decimal arithmetic" (with E. E. Swartzlander, Jr.), submitted Jan. 2019.

Dec. 2009 "A low-cost embedded SDR solution for prototyping and experimentation" (with C. R. Anderson and P. Balister), in *Proc. Software Defined Radio Technical and Product Exposition (SDR'09)*, Washington, DC, Dec. 2009.

## Licenses and Certifications

Aug. 2017 Graduate Student Member, IEEE

Dec. 2015 Professional Engineer (California)

May 2014 Most recent SSBI (TS/SCI eligible)

Sep. 2011 Amateur Radio Operator